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INFLUENCE OF SINTERING TIME ON THE MICROSTRUCTURE AND ELECTRIC PROPERTIES OF LOW-VOLTAGE ZINC OXIDE-BASED VARISTOR CERAMICS

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The results of experimental researches obtained for a varistor ceramics on the basis of zinc oxide are reported. The influence of the sintering time of the ceramics on its electric properties and microstructure is studied. The increase in the sintering time of ceramics is found to result in a broadening of the grain distribution spectrum over the grain size and in a shift of its maximum toward larger values. Specific features in the grain size distribution are revealed. It is found that, at the long-term sintering, the large grains form conductivity channels, with the barrier structure of the varistor ceramics being not destroyed, which gives rise to the growth of the real and imaginary components of the complex dielectric permittivity.

K e y w o r d s: ceramics, varistor, semiconductor, current-voltage characteristic, dielectric permittivity.

1. Introduction

Zinc oxide-based ceramics is fabricated following rather a simple traditional technology and is widely used for the manufacture of high-voltage varistors [1–3]. The fabrication of low-voltage varistors demands for more complicated and expensive technological routines. The multilayered technology is the most widespread in the mass production of radioelectronic components of this kind [4–8]. The problem of the synthesis of a low-voltage zinc oxide-based ceramics with the use of the traditional ceramic technology is actual till now and stimulates researches in this field [9–17]. It is known that a reduction of the classification voltage U_c, i.e. the voltage, at which a certain (as a rule, 1 mA [3]) current flows through the specimen, can be reached by either varying the number of intercrystalline potential barriers across the electric current flow or decreasing their height (or by controlling both those parameters simultaneously). However, the barrier height in varistor's zinc oxide ceramics depends on the composition rather weakly [18]. The reduction in the number of consecutive barriers by decreasing the specimen thickness has also technological and operational restrictions. One of the possible variants to decrease the classification voltage consists in the production of a coarse-grained varistor ceramics.

A huge number of compositions for the varistor ceramics have been synthesized and studied, and more than a thousand of them were patented [18]. However, no substantial improvement in the performance was reached in comparison with those for compositions developed as early as in the 1970s. In a significant number of works, e.g., works [19–21], the dependences of electric characteristics on the sintering temperature were studied. This technological parameter also can strongly affect the microstructure and the electric properties of ceramics. Its increase should result in the growth of grain sizes. However, the attention to such researches was paid only in a few works [22]. Proceeding from this fact, this work was aimed at analyzing the influence of the sintering time on

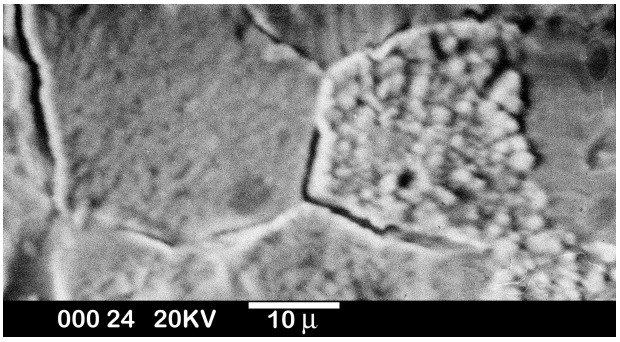

Fig. 1. Micrograph of a ceramic slice (the sintering time is 1 h)

the electric properties and the microstructure of low-voltage varistor ceramics ZnO–Bi_2O_3–TiO_2–MnO_2–CoO–NiO.

2. Experimental Part

2.1. Specimens

Specimens of the varistor ceramics with the composition ZnO–Bi_2O_3–TiO_2–MnO_2–CoO–NiO were fabricated following the standard technology [23]. The latter included the oxide batching, wet mixing, drying, and pressing disks 8 mm in diameter and 2 to 3 mm in thickness. The content of zinc oxide in the blend was 95 wt.%. Sintering was carried out in air at a temperature of 1473 K. The sintering time was varied in the interval from 1 to 24 h. Electrodes were deposited onto the specimens with the help of the liquid indium-gallium eutectics.

For microstructure researches, ceramics slices were obtained. The specimens were treated using silicon carbide powders (the crystal size from 40 to 1 μm) on glass. The final polishing was made with the help of a diamond paste with the dimension of crystals smaller than 0.1 μm. After degreasing, the surface was etched using a 10% aqueous solution of HCl. The etching time varied from 10 to 30 s.

2.2. Measurement technique

The microstructure of ceramic specimens was analyzed on a raster electron microscope REM-106I (SELMI, Ukraine). The grain sizes in slices were measured, by using the method of secants. The maximum visible dimension of a grain, d, was estimated. While analyzing the distribution of grains in the slices over their dimensions, the total number of objects, whose size was estimated, n_Σ, varied from 150 to 250 for every specimen. The number of grains within the certain i-th interval of linear dimensions (n_i, where $i = 1, 2, ...$) was counted. The grain size increment amounted to 5 μm at that; i.e. n_1 is the number of grains in the slice with the dimensions less than or equal to 5 μm, n_2 is the number of grains with the dimensions more than 5 μm but less than or equal to 10 μm, and so on.

The current-voltage characteristics (CVCs) were measured with the use of industrial devices: digital voltammeters B7-27A/1 and B7-35, and controllable constant voltage sources TV-3 and TV-42. The coefficient of CVC nonlinearity β was determined in the interval of current densities through the specimen from 0.1 to 1 mA/cm^2 by the formula [9, 24]

$$\beta = \frac{\lg J_1/J_2}{\lg E_c/E_2},$$

where $J_1 = 1$ mA/cm^2, $J_2 = 0.1$ mA/cm^2, and E_c and E_2 are the corresponding electric field strengths.

The real (ε') and imaginary (ε'') parts of the complex dielectric permittivity were measured at a frequency of 100 kHz with the help of a capacitance and quality factor meter BM-560.

3. Results and Their Discussion

3.1. Microstructure

The fabricated ceramics had a polycrystalline structure typical of sintered metal oxides (Fig. 1) [25]. In Fig. 2, the normalized distributions of grains over their size d in the varistor ceramics are demonstrated for various sintering times. In the ceramics sintered for 1 h, the maximum grain size did not exceed 70 μm (Fig. 2, *a*). The distribution maximum takes place within the grain size interval from 5 to 10 μm. One should also pay attention that another smaller maximum is observed in the interval from 50 to 55 μm.

The increase of the sintering time expectedly [26] resulted in a growth of grain sizes and, accordingly, a broadening of the grain size distribution spectrum, and a shift of its maximum toward larger d (Fig. 2). The average size of grains, $\bar{d}$, did not change essentially at the sintering times up to 8 h inclusive, amounting to about 20 μm (Fig. 3). Nevertheless, there appeared separate crystallites about 100 μm in dimension (Fig. 2, *b*) in the ceramics synthesized for

4 h and longer, and about 200 μm in the ceramics sintered for 24 h.

Such a character of the spectrum modification can testify to the appearance of large grains, mainly owing to the merging of two smaller ones with half as large linear dimensions. The merging of a large grain with a grain that is several times smaller does not give rise to an appreciable increment in the volume of the large grain. We could assume that, when two grains merge together, only their volumes rather than linear dimensions should be summed up. However, it should be taken into account that, when grains agglomerate owing to their sintering at temperatures substantially lower than the melting temperature of the basic ceramic substance (e.g., the temperature of ZnO sublimation equals 2073 K [27]), the motion of their intercrystalline interfaces is hindered by the matrix of surrounding grains. Admixtures insoluble in the basic substance behave analogously at sintering [28]. Therefore, the grain cannot minimize its free energy.

The average grain size grew from 21 to 36 μm, when the sintering time was increased from 1 to 24 h (Fig. 3).

3.2. Electric properties

The current-voltage characteristics of specimens are depicted in Fig. 4. Despite some spread of parameters typical of inhomogeneous materials [29], the measured CVCs can conditionally be divided into 3 groups: (*a*) specimens sintered for less than 4 h are characterized by a low conductivity in the weakly nonlinear section and have a highly nonlinear section in the interval of electric field strengths from 55 to 70 V/mm; (*b*) specimens sintered for 6 to 12 h are characterized by a higher conductivity in the weakly nonlinear section and have a highly nonlinear section in the interval of electric field strengths from 45 to 60 V/mm; and (*c*) specimens sintered for more than 12 h are characterized by a high conductivity and have almost linear CVCs.

From Fig. 4, we can obtain the dependences of the electric field strength E_c at a classification current of 1 mA/cm^2 through the specimen (Fig. 5, *a*) and the coefficient of CVC nonlinearity β (Fig. 5, *b*) on the sintering time. At the sintering time up to 12 h inclusive, the field strength first increases from 60 V/mm at 1 h to 70 V/mm at 4 h, then it decreases

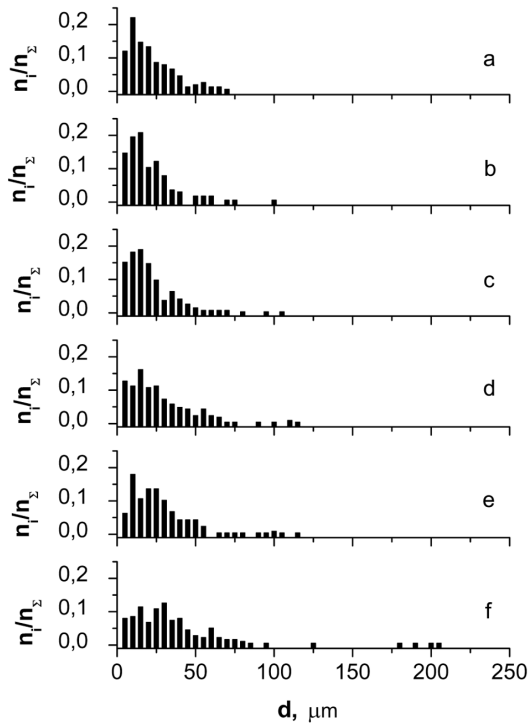

Fig. 2. Distributions of the relative number of grains over sizes in the ceramics for various sintering times: 1 (*a*), 4 (*b*), 8 (*c*), 12 (*d*), 16 (*e*), and 24 h (*f*)

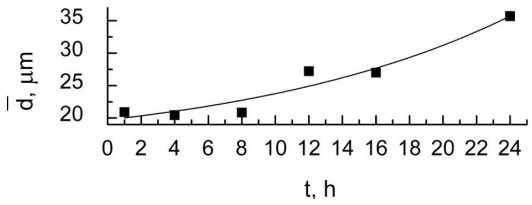

Fig. 3. Dependence of the average grain sizes in the ceramics on the sintering time

to 52 V/mm at 12 h, which can be explained by processes that run in the intercrystalline phase of the ceramics – in particular, the evaporation of Bi_2O_3 – and by the growth of the average grain size. The corresponding nonlinearity coefficient changes in the interval from 18 to 28. A further increase of the sintering time results in a drastic change of the electric specimen characteristics: the nonlinearity of specimen CVCs diminishes, their form approaches the ohmic one (Fig. 4), so that the nonlinearity coefficient decreases to values of 1 to 2, and the field strength at the classification current falls to 2–6 V/mm. Hence,

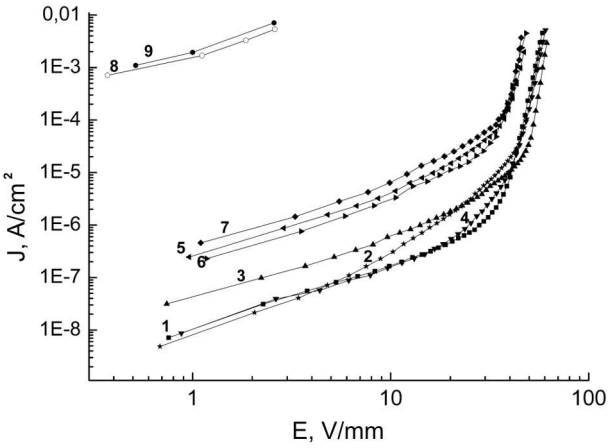

Fig. 4. Current-voltage characteristics for a specimen of the varistor ceramics sintered for various times: 1 (*1*), 2 (*2*), 3 (*3*), 4 (*4*), 6 (*5*), 8 (*6*), 12 (*7*), 16 (*8*), and 24 h (*9*)

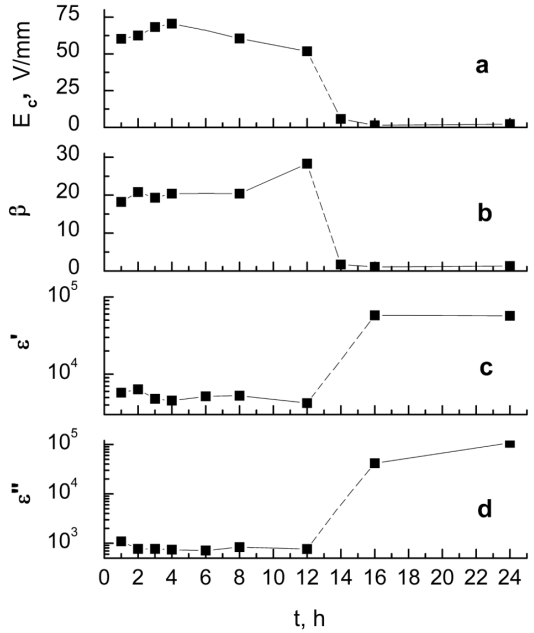

Fig. 5. Dependences of the electric field at the classification voltage across a specimen (*a*), the CVC nonlinearity coefficient (*b*), and the real (*c*) and imaginary (*d*) parts of the complex dielectric permittivity (at $f = 10^5$ Hz) on the sintering time

by their electric properties, the specimens can be divided rather neatly into two large groups: (1) sintered for up to 12 h inclusive and (2) sintered for a longer time.

The drastic CVC modification at the sintering for more than 12 h can be explained by the formation of "superlarge" grains with the dimensions of about 100 and 200 μm in the ceramics structure (Fig. 2), the number of which is sufficient for the emergence of continuous conductivity channels through them. However, no destruction in the symmetric-barrier structure of varistors seems to take place at that, which is confirmed by the values of real and imaginary parts of the complex dielectric permittivity (Figs. 5, *c* and *d*). For group 1, $\varepsilon' = (4.5 \div 6.4) \times 10^3$ and $\varepsilon'' = (7 \div 10.8) \times 10^2$, which is typical of the varistor ceramics [19,30,31]. For the specimens of group 2, ε' and ε'' are much larger: $\varepsilon' = (5.7 \div 5.8) \times 10^4$ and $\varepsilon'' = (4.2 \div 10.8) \times 10^4$. This fact testifies to a drastic growth of the capacity and the conductivity of specimens at sintering times longer than 12 h. The increase of ε'' correlates well with the CVCs of those specimens. It is known [32] that the high capacity and, accordingly, the large values of ε' in the varistor ceramics are associated with the migration mechanism of polarization. The grains in the varistor ceramics, except for thin (0.3–2 nm [33]) regions of intergrain phases, possess a high conductivity [1, 2, 25], but are separated by intercrystalline potential barriers that electrically insulate them from one another. The thickness D of this semiconductor layer depleted of charge carriers can be estimated as

$$D = \frac{\varepsilon_0 \varepsilon \varphi_s}{e^2 n_{\mathrm{d}}},$$

where ε_0 is the electric constant, ε the dielectric permittivity of zinc oxide, e the electron charge, n_{d} the donor concentration, and φ_s the barrier height [34].

Using the formula for the plane capacitor, the capacity of this structure

$$C = \frac{\varepsilon_0 \varepsilon S}{2D},$$

where S is the contact area of grains. Hence, a structure similar to capacitors connected in series is formed along the way of the electric current flow. A strong reduction in the number of those capacitors owing to the emergence of "superlarge" grains results in the growth of the real part of the complex dielectric permittivity. Those speculations are confirmed by the nonlinear increase of the capacity of varistor ceramics specimens at a reduction of their thickness [35]. At the same time, if the barrier structure had been destroyed and the grain had contacted directly with one

another without the participation of intercrystallite potential barriers, ε' would have tended to a value of about 10, which is typical of single-crystalline ZnO [27, 36].

A drastic decrease of the CVC nonlinearity coefficient for specimens with the sintering time exceeding 12 h can be explained by the fact that even the lowest values of the applied voltage turn out enough for overcoming a few barriers formed between "superlarge" grains. Moreover, the height of those barriers can be substantially lowered owing to a gradual escape of bismuth oxide from the intergrain phase in the course of sintering.

4. Conclusions

Experimental researches carried out for the varistor ceramics on the basis of zinc oxide testifies to the dependence of the electric properties of those materials on their microstructure. The increase of the ceramics sintering time results in a broadening of the grain size distribution spectrum and a shift of its maximum toward larger values. Large grains mainly appear owing to the merging of two smaller ones with the linear dimensions half as large.

At large sintering times, the conductivity channels are formed through large grains without the destruction of the barrier structure in the varistor ceramics, which results in a substantial growth of both the real and imaginary components of the complex dielectric permittivity and, accordingly, gives rise to the formation of a material possessing a high conductivity and a large capacity. In order to optimize the properties of the low-voltage varistor ceramics, the sintering time has to be prolonged to 10–12 h, which results in a reduction of the classification voltage, a growth of the CVC nonlinearity coefficient, and an increase of the average grain size. However, the value of optimum sintering time can be specific, by depending on the ceramics composition.

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ВПЛИВ ТРИВАЛОСТІ СПІКАННЯ НА МІКРОСТРУКТУРУ І ЕЛЕКТРИЧНІ ВЛАСТИВОСТІ НИЗЬКОВОЛЬТНОЇ ВАРИСТОРНОЇ КЕРАМІКИ НА ОСНОВІ ОКСИДУ ЦИНКУ

Р е з ю м е

Наведено результати експериментальних досліджень варисторної кераміки на основі оксиду цинку. Вивчено вплив тривалості спікання кераміки на її електричні властивості і мікроструктуру. Встановлено, що збільшення часу спікання кераміки призводить до розширення спектра розподілу зерен за розмірами і зрушення максимуму в область більших значень. Виявлено специфічні особливості розподілу зерен за розмірами. При тривалому спіканні відбувається утворення каналів провідності по великих зернах без руйнування бар'єрної структури варисторної кераміки, що приводить до збільшення дійсної і уявної складових комплексної діелектричної проникності.