SILICON p-MOS AND n-MOS TRANSISTORS WITH UNIAXIALLY STRAINED CHANNELS IN ELECTRONIC DEVICE NANOTECHNOLOGY

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The effect of uniaxial stress on the mobility of charge carriers in n-Si and p-Si crystals used for the fabrication of n-MOS and p-MOS transistors is considered. The stress dependences of the longitudinal and transverse tensoresistive effects in p-Si obtained for the principal crystallographic orientations ($X \parallel [100]$, $X \parallel [110]$, and $X \parallel [111]$) are presented. An abrupt decrease of the longitudinal tensoresistive effect in p-Si with increasing stress is due to a reduction of the longitudinal effective mass of heavy holes and the corresponding rise of their mobility. In n-Si, a growth of the uniaxial stress $X \parallel [100]$ results in the complete removal of f-transitions from intervalley scattering under a large energy splitting of single-type Δ_1-valleys ($\Delta\varepsilon > 10$ kT), which leads to an increase of the electron mobility in the temperature range 78–300 K. The change of g-transitions under the splitting of single-type Δ_1 valleys in this temperature interval has no effect on the electron mobility. We also describe technological developments used by "Intel Corporation" for the fabrication of integrated circuits with uniaxially strained channels of MOS transistors.

1. Introduction

As is known, the mobility of charge carriers determines such important characteristics of transistors as the slope of volt-ampere characteristics (VACs) and their limiting switching frequency [1, 2]. In this work, we consider the use of uniaxial deformation for the increase of the mobility of charge carriers (electrons and holes) in silicon representing the basic material for the fabrication of integrated circuits for today. For this purpose, we present the dependences of the longitudinal and transverse tensoresistive (TR) effects obtained for all principal crystallographic directions in p-Si ($X \parallel [100]$, $X \parallel [110]$, and $X \parallel [111]$) and for the crystallographic direction $X \parallel [100]$ in n-Si, at which f-transitions are completely removed from the intervalley scattering under strong uniaxial stresses. In addition, the mechanisms responsible for some regularities of the TR effects will be described and the possibilities of the further increase of the mobility at the expense of the uniaxial elastic deformation of channels of p-MOS and n-MOS silicon transistors will be demonstrated.

2. Experimental Results and Their Discussion

Based on experimental data, let us investigate the effect of strong uniaxial deformation of p-Si and n-Si crystals.

Figures 1–3 present the specific resistances of p-Si crystals as functions of the uniaxial stress, i.e. the longitudinal and transverse TR effects, at various orientations of the stress X relative to the principal crystallographic directions [3]. In the case of the longitudinal TR effect, one observes a decrease of the specific resistance of crystals with increasing stress for all orientations, which is caused by a reduction of the effective mass of heavy holes resulting in the rise of their mobility in the direction of uniaxial deformation. The effective hole mass changes due to the reconfiguration of the valence band (Fig. 4) under the influence of the strong uniaxial stress [4]. In this case, the deformed isoenergetic spheres in non-deformed p-silicon are transformed to flattened ellipsoids (in the region of heavy holes) or prolate ellipsoids (in the region of light holes).

The increase of the electron mobility in uniaxially strained n-silicon crystals is caused by quite a different reason. Here, one should consider the relative contribution made to the intervalley scattering by f- and g-transitions. The data of measurements of both the longitudinal TR effect at $X \parallel [100] \parallel E$ and the transverse one at $X \parallel [100] \perp E$ (Fig. 5) have definitely proved the determinative role of f-transitions and an insignificant

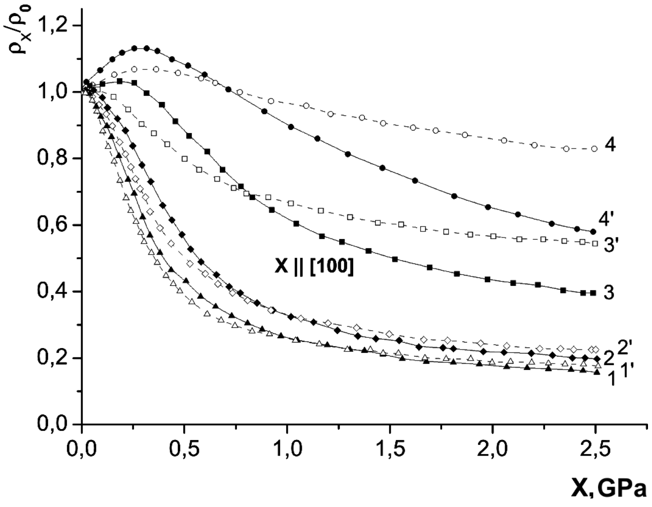

Fig. 1. ρ_x/ρ_o as functions of the uniaxial stress $X\|[100]$ for p-Si(B) at various concentrations of the boron impurity (m^{-3}): *1* – $N_{\mathrm{B}} = 4.8\times10^{18}$, *2* – 2.5×10^{19}, *3* – 9.1×10^{21}, *4* – 2.3×10^{22}. $T = 78$ K. Dotted lines correspond to $X\|[100]\perp E$, solid lines – to $X\|[100]\|E$

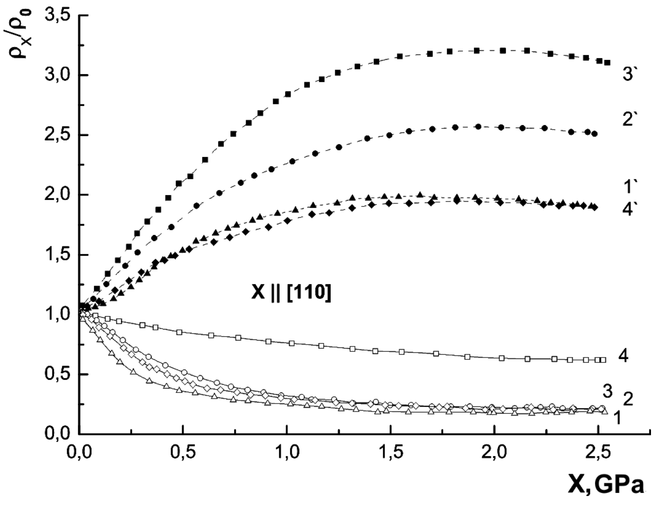

Fig. 2. ρ_x/ρ_o as functions of the uniaxial stress $X\|[110]$ for p-Si(B) at various concentrations of the boron impurity (m^{-3}) : *1* – $N_{\mathrm{B}} = 4.8\times10^{18}$, *2* – 2.5×10^{19}, *3* – 9.1×10^{21}, *4* – 3.1×10^{24}. $T = 78$ K. Dotted lines correspond to $X\|[110]\perp E$, solid lines – to $X\|[110]\|E$

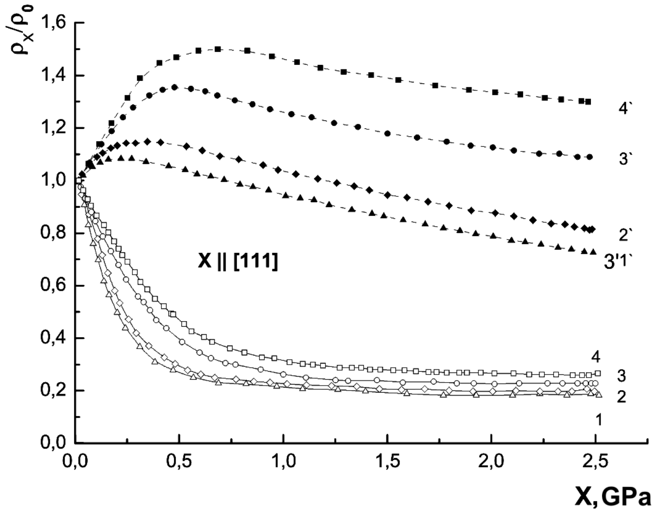

Fig. 3. ρ_x/ρ_o as functions of the uniaxial stress $X\|[111]$ for p-Si(B) at various concentrations of the boron impurity (m^{-3}): *1* – $N_{\mathrm{B}} = 4.8\times10^{18}$, *2* – 2.5×10^{19}, *3* – 9.1×10^{21}, *4* – 2.3×10^{22}. $T = 78$ K. Dotted lines correspond to $X\|[111]\perp E$, solid lines – to $X\|[111]\|E$

role of g-transitions in the intervalley scattering in the temperature range 100–300 K. That is why, at strong stresses $X\|[100]$ and $T = 300$ K, at which f-transitions are completely removed from the intervalley scattering (under the condition $\Delta\varepsilon > 10$ kT), the electron mobility in silicon grows due to the direct decrease of the electron scattering. The dominant contribution made to the intervalley scattering by f-transitions at strong uniaxial stresses was first demonstrated by the example of the temperature dependences of the longitudinal TR effect in n-silicon [5]. More than 30 years later, "Intel" has practically adopted this fundamental discovery in such large-scale form.

Strong stresses ($X > 5$ GPa) in uniaxially strained n-Si in the [111] direction result in a metal-nonmetal transition caused by the square increase of the effective electron mass with the stress. To describe the stress dependence of the effective mass, we used the following relations. It is known that, in the region of the metal-nonmetal transition, the conductivity of a degenerate semiconductor is determined by the expression

$$\sigma_x = \sigma_0[n/n_c(x)]^\gamma\,, \tag{1}$$

where n is the impurity concentration in the degenerate semiconductor, and $n_c(X)$ is the critical concentration for the metal-nonmetal transition depending on the uniaxial stress that can be presented in the form [6]

$$n_c(X) = n_c(0)(m_x^*/m_0^*)^3. \tag{2}$$

Let us expand the stress dependence of the effective electron mass m^* in a series in terms of the stress

$$m_x^* = m_0^*(A + BX + CX^2 + ...). \tag{3}$$

Restricting ourselves to the linear and square terms and substituting this nonlinear dependence (caused by

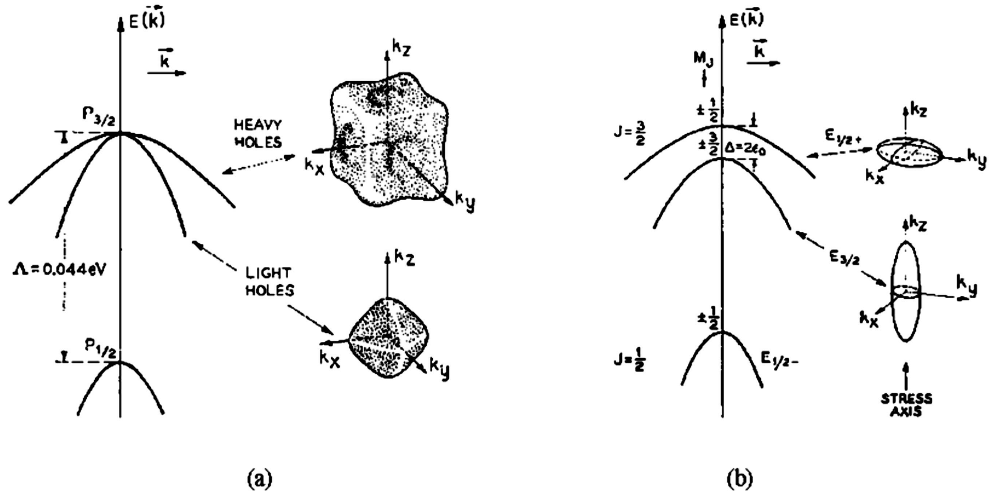

Fig. 4. Valence band structure for non-deformed (a) and uniaxially strained (b) silicon and germanium crystals

the splitting of the energy bands at the edge of the Brillouin zone) into Eq. (2), we obtain

$$\sigma_x = \sigma_0 [\frac{n}{n_c(0)(A+BX+CX^2)^3}]^\gamma, \qquad (4)$$

where $A = n/n_c$, B, and C are fitting parameters, γ is some parameter determined to a good accuracy in a number of works (see, e.g., [7]). Comparing the experimental data with the corresponding stress dependence of σ_x (4) (only for the region of metal conductivity), we have found that, in strongly degenerate crystals, the stress dependence of the effective mass is determined solely by the square term. It is worth noting that namely the square dependence of the variation of the effective electron mass in silicon at $X \| [111]$ is responsible for the metal-insulator transition in degenerate crystals at the further increase of X as $T \to 0$.

The application of strong uniaxial stresses also allowed us to determine the mechanisms of the TR effects in neutron-doped silicon. It is established that the peculiarities of the longitudinal TR effect are related to technological thermal donors necessarily arising in the bulk of crystals at their technological annealing (2 h, $T \approx 800$ °C). That is why crystals of neutron-doped silicon should be designated as Si(P,TD), because thermal donors determine the majority of the properties of such crystals and cardinally change the temperature dependences of their resistance (conductivity). For comparatively pure crystals doped with phosphorus impurity from a melt, the temperature dependence of the resistance in the range 78–300 K is determined by the metal type of conduction (resistance grows with increasing temperature). Whereas, for similar silicon crystals doped with phosphorus by the neutron doping technique, the resistance significantly decreases with the temperature increasing in the same range (dependence typical of a semiconductor). Certainly, the Hall parameters of crystals also change in this case. In addition (as was already mentioned), the TR properties of silicon crystals neutron-doped with phosphorus also qualitatively change.

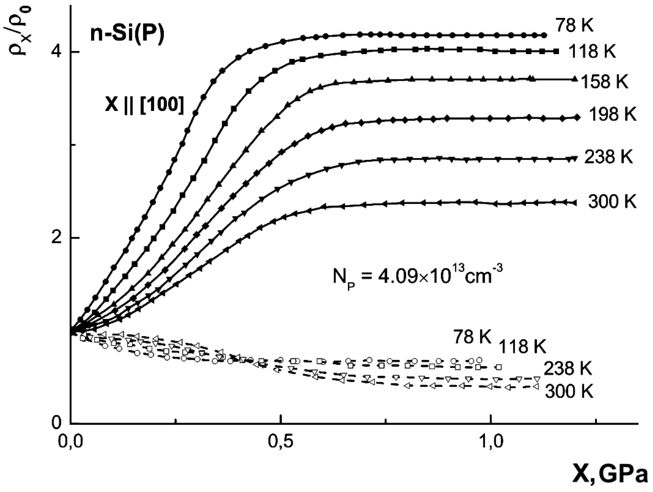

Fig. 5. ρ_x/ρ_o as functions of the uniaxial stress $X \| [100]$ for n-Si(P) at various temperatures. Solid curves correspond to $X \| [100] \| E$, dotted curves – to $X \| [100] \perp E$

3. "Intel Corporation" Nanotechnologies Used for Producing Integral Circuits with Uniaxially Strained Channels of MOS Transistors

The described reconfiguration of the valence and conduction bands under the conditions of strong uniaxial stresses is technologically and constructively reached in the following way. First, an intermediate $\mathrm{Si}_{1-y}\mathrm{C}_y$ or $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layer is epitaxially deposited on a silicon substrate. After that, a silicon channel layer is deposited in the same way. This layer will be subjected to a compressive or stretching deformation, whose magnitude can be varied by changing the composition of the intermediate layers.

Let us consider how "Intel" is planning to proceed from the 90-nm technology to the 65-nm one and then to the 45-nm and 32-nm technologies. First, we discuss which features of the old technology will remain in a new one. First of all, it is 300-mm silicon plates for substrates. The lithographical equipment used for the 90-nm technology will also most probably remain (we mean the lithographical equipment with 193-nm argon-fluoride lasers earlier used for the fabrication of 90-nm chips). This technology has acquired a good reputation with the 90-nm technological process and can be used for the 65-nm one with some improvements of the photoresistor material. Being still far from the practical adaptation of extreme ultraviolet lithography, "Intel Corporation" uses facilities and technologies successfully employed in the previous technological processes.

Now, let us find out the advantages provided by the technology of uniaxially strained silicon for the first time used in full by "Intel". The channel of a unipolar p-MOS transistor is subjected to a uniaxial compressive deformation with the help of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ solid solution epitaxially deposited into dips etched opposite the channel, whereas the stretching deformation in the channel of an n-MOS transistor is created with the help of a stretching nickel silicide film epitaxially deposited above the transistor gate. At room temperature, this results in the almost twofold increase of the electron mobility. The growth of the hole mobility (at room temperature and a uniaxial stress of ≈ 600 MPa) amounts to 40%.

The use of the uniaxial deformation of silicon and the transition to the 65-nm technology allow one to improve one of the most critical parameters of the up-to-date processor – the transistor leakage current that decreases almost by four times.

In addition, the reduction of the gate length to 35 nm and the thickness of the oxide layer to 1.2 nm has made it possible to decrease the gate capacity by approximately 20%, which results in the growth of the switching frequency by a factor of 1.4 and reduces the active energy consumption of a chip.

The transition from the 90-nm technological process to the 65-nm one provides the twice denser arrangement of transistors on the same area. This tendency will conserve when passing to the 45-nm and 32-nm technological processes. Particularly, if using the 45-nm technology, an area of 100 mm^2 will contain one billion transistors, whereas the use of the 32-nm technology allows one to arrange two billions of them.

Another basic problem of optimizing the operation of transistors is the energy consumption by chips. The main method to decrease the energy consumption employed by "Intel Corporation" is the use of the so-called "sleeping transistors". Memory blocks not used at the moment are completely disconnected from the power supply, which allows one to decrease the leakage current approximately threefold.

Thus, one can consider that the use of uniaxially strained silicon accompanied by the increase of the carrier mobility allows one to noticeably improve the basic characteristics of devices. The technology of uniaxially strained channels of silicon p-MOS and n-MOS transistors will be employed as long as silicon will be employed in the device production technology.

In addition, it is worth noting that the technology of uniaxially strained channels of transistors uses epitaxial techniques. One can say that all the nanotechnology of uniaxially strained silicon is based on epitaxy that allows one to obtain perfect layers of semiconductor materials, their alloys, and structures.

A similar technology of uniaxial deformation of channels of p-MOS and n-MOS transistors is also used in "semiconductor on insulator" structures [8]. Uniaxial compressive and stretching deformations of channels of such transistors will be realized due to the epitaxial deposition of $\mathrm{Si}_{1-y}\mathrm{C}_y$ or $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ alloys (for uniaxial compressive and stretching deformations, respectively) into dips epitaxially etched opposite to channels.

4. Conclusions

The mechanisms of the measured longitudinal and transverse TR effects are determined both in p-Si (for the principal crystallographic directions $X \| [100]$, $X \| [110]$, and $X \| [111]$) and in n-Si (for the crystallographic direction $X \| [100]$).

In p-Si, these mechanisms are related to the reconfiguration of the valence band under the action of a uniaxial stress, which results in the transformation of deformed isoenergetic spheres (in non-deformed crystals) into ellipsoidal isoenergetic surfaces formed under strong uniaxial stresses. A large anisotropy of these isoenergetic surfaces causes a strong anisotropy of the longitudinal TR effect with respect to the transverse one, which allows one to find the directions that determine the increase of the mobility of heavy holes due to a considerable reduction of their effective mass along the direction of the stress.

In n-Si, the strong uniaxial stresses $X \| [100]$, at which f-transitions are completely removed, result in an increase of the electron mobility, which causes a relative increase of the mobility in the case of the longitudinal TR effect and its absolute increase in the case of the transverse one. In this case, the effective electron mass changes from $m_c = 3m_0/2K_m + 1 = 0.26m_0$, where K_m is the parameter of the effective mass anisotropy, to $m_l^* = 0.91m_0$ (for the longitudinal TR effect) and to $m_\perp^* = 0.19m_0$ (for the transverse TR effect). In other words, we observe the absolute increase of the mobility in the case of the transverse TR effect.

The work presents the results of technological developments used by “Intel Corporation” to obtain uniaxial stresses in channels of p-MOS and n-MOS transistors. The applied epitaxial technologies allow one to obtain perfect layers of alloys of various semiconductors ($\mathrm{Si}_{1-y}\mathrm{C}_y$, $\mathrm{Si}_{1-x}\mathrm{Ge}_x$) and “semiconductor on insulator” structures.

It is worth adding that only strong uniaxial stresses make it possible to reach such a large increase of the mobility of charge carriers ($\approx 40\%$ – for holes in p-MOS transistors and $\approx 200\%$ – for electrons in n-MOS transistors) at stresses of 600–700 MPa. Neither biaxial deformation nor hydrostatic stress can lead to such noticeable changes of the carrier mobility.

The advantages of the method of strong uniaxial stresses realized with the help of an original set-up [9] as compared to the method of weak uniaxial stresses (Smith piezoresistance [10]) are described.

It is also worth noting that, using the method of strong uniaxial stresses, we have determined more than 15 parameters for the conduction bands of silicon and germanium, including fundamental ones and those determined for the first time (for example, the parameters Δ_1 of valleys of the C-band in germanium).

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КРЕМНІЄВІ p-МОН ТА n-МОН ТРАНЗИСТОРИ З ОДНОВІСНО ДЕФОРМОВАНИМИ КАНАЛАМИ У НАНОТЕХНОЛОГІЇ ЕЛЕКТРОННИХ ПРИЛАДІВ

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Резюме

Розглянуто вплив одновісного тиску на рухливість носіїв струму у кристалах n-Si та p-Si, який використовується при виготовленні n-МОН та p-МОН транзисторів. Представлено залежності поздовжнього і поперечного тензорезистивних (ТР) ефектів, отримано у кремнії p-типу для головних кристалографічних орієнтацій $X \| [100]$, $X \| [110]$, $X \| [111]$. Стрімке зменшення поздовжнього ТР ефекту в p-Si зі збільшенням тиску пов’язано із зменшенням поздовжньої ефективної маси важких дірок і відповідним збільшенням їх рухливості при зростанні X. У кремнії n-типу зі збільшенням одновісного тиску $X \| [100]$ відбувається повне усунення f-переходів з міждолинного розсіювання при великому енергетичному розщепленні однотипних Δ_1-долин ($\Delta\varepsilon > 10$ kT), що веде до зростання при цьому рухливості електронів у температурному інтервалі 78–300 K. На величину рухливості електронів у цьому температурному інтервалі зміна g-переходів при розщепленні однотипних Δ_1 долин не впливає. Крім того, наведено технологічні розробки, які використовує фірма “Intel Corporation” при виробництві інтегральних мікросхем з одновісно-деформованими каналами МОН транзисторів.